analog dialogue

A forum for the exchange of circuit technology: Analog and Digital, Monolithic and Discrete

10-BIT MONOLITHIC CMOS D/A CONVERTER

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High-Precision Thin-Film Resistor Networks

Op Amps — How Fast is Fast?

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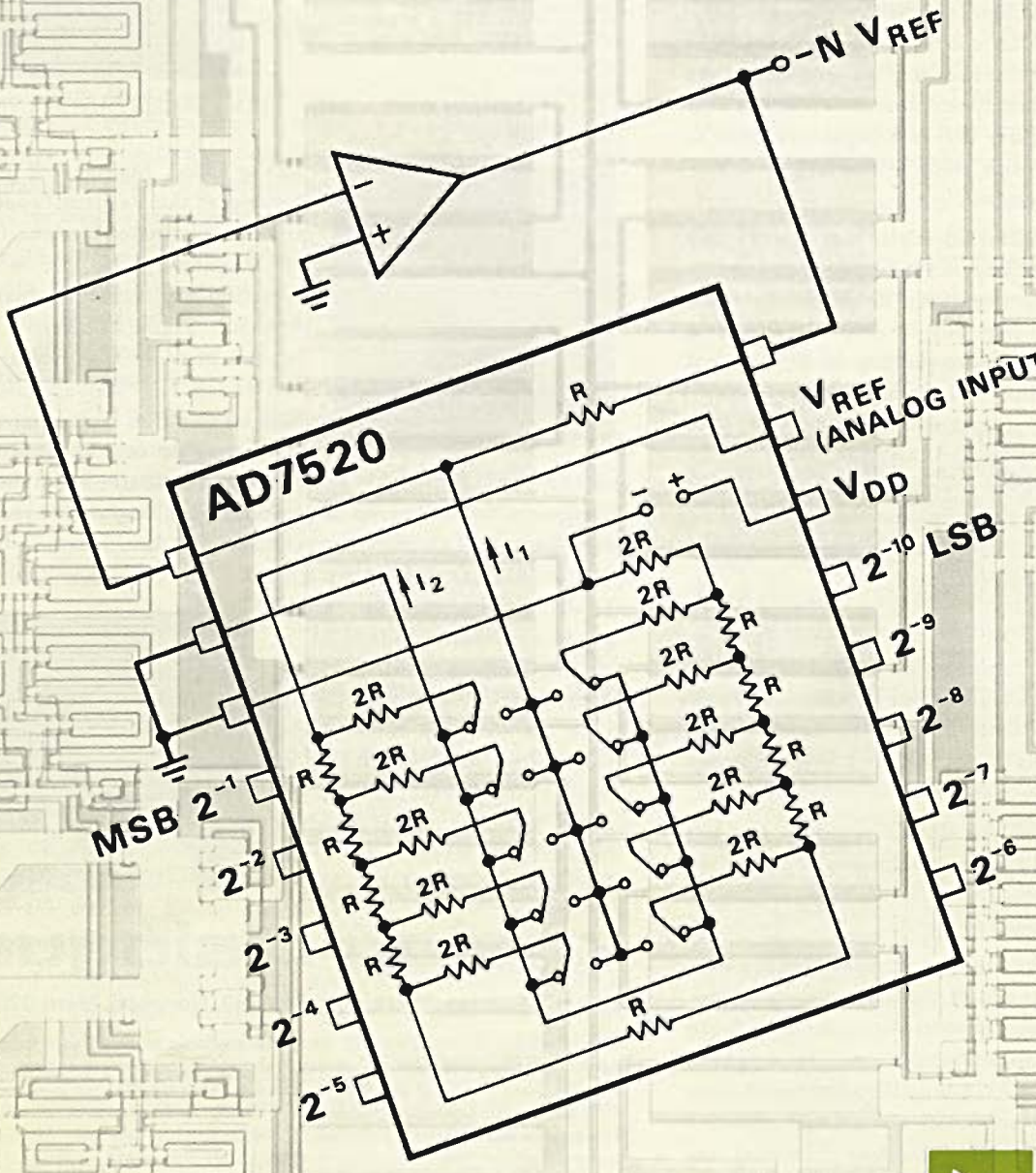

Volume 8, No. 1

ANALOG DEVICES

Editor's Notes

The integrated-circuit art has reached the state at which the general reaction to the introduction of a new device can scarcely be termed "excitement," however unique, valuable, or unprecedented the circuit. We've become jaded by too many breakthroughs; the miracle of the I.C. has already joined the miracle of the transistor and the miracle of the vacuum tube in the limbo of "history." Fortunate are we who have lived through all three eras and can still retain the sense of wonder!

Despite its unglamorous designation (except perhaps to a dedicated numerologist), the AD7520 digital-to-analog converter is one of the many milestones in integrated-circuit technology. It is the first major circuit to combine CMOS circuitry and thin-film resistors on a single chip. It is the first commercially-available 10-bit monolithic D/A converter to employ CMOS processing. Above all, to the extent that we can determine from a close watch of the marketplace, it seems to be the first monolithic 10-bit D/A converter that is being produced with high yields, at low cost, and with ready availability to all purchasers, in realistic quantities, *now*.

A major reason for its successful advent is that it was really designed with the *user* in mind. The user is free to choose an op amp that will produce the performance he desires (and the 500ns settling time will challenge any op amp); he is free to choose a reference that will have the stability he desires (and the 10ppm/°C *max* specification will challenge any reference); and he is free to use it as a 4-quadrant multiplying DAC with response well up into the ultrasonic range. In other words, rather than seek a technological *tour de force*, with all the bells and whistles, we sought a practical device that could be easily produced, purchased, and used -- and it turned out to be a technological *tour de force* nevertheless!

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WHERE WE'RE GOING

We've steadfastly sought to maintain this journal as a reflection of the technical aspects of the business of Analog Devices: our products – old and new: their design, applications, implications, and specifications, plus interpretations of the influence of advancing technology on the technical interests of our users.

Just as steadfastly, we've sought to avoid discussions of a less technical nature, since our audience is presumed to be interested principally in how we can help them use the new techniques and products to solve their design problems.

Well, you can't help noticing that our products continually span a wider range, both of markets and of manufacturing technologies. If you're interested in learning more about the underlying philosophy (and some of the recent results), we'd be delighted to send you a copy of our 1973 Annual Report, which goes into those matters (and justly so) in far more satisfying detail than is within the charter of *Analog Dialogue*. You may use the reply card to request it.

▶▶▶

Dan Sheingold

THE AUTHORS

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Jim Cecil, Engineering Manager at ADI/California, is the designer of the AD7520 d/a converter. He has degrees in E.E. from both Arizona State and the University of Arizona, successful integrated-circuit DAC and op amp designs, 2 patents in d/a converter design, and several years with Motorola. He now has engineering responsibility for the CMOS product line at Analog Devices.

Gerald "Jerry" Whitmore obtained his basic engineering education at Eastern Montana College and Diablo Valley College, plus varied and relevant engineering experience in the U.S. Navy and at Zeltex. He is now an Applications Engineer at ADI/California.

"HIGH PRECISION THIN-FILM RESISTANCE NETWORKS," p. 6

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A 10-BIT MONOLITHIC CMOS D/A CONVERTER THAT CAN BE USED FOR 4-QUADRANT MULTIPLICATION

by Jim Cecil and Jerry Whitmore

The AD7520* is a 10-bit multiplying digital-to-analog converter constructed on a single silicon chip. It consists of 10 CMOS (complementary metal-oxide-semiconductor) switches and a thin-film-on-CMOS R-2R ladder network. The digital input, which responds to the wide voltage swings of CMOS logic, is also compatible with TTL/DTL logic levels. Two complementary current outputs are available for use with inverting operational amplifiers.

Besides the 10-bit resolution, the AD7520 family has maximum nonlinearities as low as ±0.05% of V_{REF}, nonlinearity temperature-coefficient of 2ppm/°C, and maximum feedthrough error of ½ least-significant bit (LSB = 0.1%) at 100kHz. Typical settling time following a full-scale digital input change is 500ns.

In addition to a constant or variable reference (current or voltage), of either positive or negative polarity, the AD7520 requires one external operational amplifier for unipolar digitally-set gains (2-quadrant multiplication) or two amplifiers for bipolar gains (4-quadrant multiplication).

The 74 x 96 mil (1.88 x 2.44mm) chip, normally housed in a 16-pin hermetically-sealed ceramic dual in-line package, can also be made available in a flatpack or plastic DIP. It will operate from a single +5 or +15V power supply, and it dissipates only 20mW, including the ladder network.

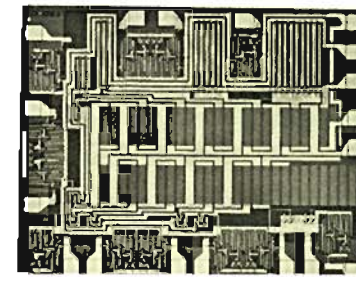
It can be used for D/A and A/D conversion, multiplication and division, programmable power supplies, digitally-programmed filters, and digital-analog function generation. Besides unipolar conversion (of either polarity), offset-binary, two's-complement, and sign-magnitude bipolar operation can also be implemented.

ADVANTAGES OF CMOS D/A CONVERSION

Commercially-available monolithic D/A converters have been, as of this writing, principally processed by conventional bipolar linear processing by conventional bipolar linear processing techniques. While 6- and 8-bit converters have been easily achievable, 10-bit conversion has been more difficult to obtain with good yields (and low cost) because of the finite β of the switching devices, the V_{BE}-matching requirement, the matching and tracking requirements on the resistance ladders, and the tracking limitations caused by the thermal gradients produced by high internal power dissipation.

All of these problems can be solved or avoided with CMOS devices. They have nearly-infinite current gain, eliminating β problems. There is no equivalent in CMOS circuitry to a bipolar transistor's V_{BE} drop; instead, a CMOS switch in the *on* condition is almost purely resistive, with the resistance value controllable by device geometry. The temperature-tracking problems of diffused resistors were solved easily: they weren't used.

*For complete information on the AD7520, use the reply card. Request **L1**.



The R-2R ladder is composed of 2kΩ/square silicon-chromium resistors (a 10kΩ resistor has a very manageable length/width of 5:1), deposited on the CMOS die. While the absolute temperature coefficient of these resistors is 150ppm/°C, their tracking with temperature is better than 1ppm/°C. The feedback resistor for the output amplifier is also provided on the chip, to ensure that the DAC's gain-temperature coefficient is better than 10ppm/°C by compensating for the absolute temperature coefficient of the network.

Finally, the low on-chip dissipation of only 20mW (including the dissipation of the ladder network), in conjunction with the excellent tracking capabilities of the thin-film resistors, minimizes linearity-drift problems caused by internally-generated thermal gradients. It also helps to minimize the power and cooling requirements for circuitry that the AD7520 is used in.

(continued on p. 4)

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Figure 1 shows a functional diagram of the D/A converter, which employs an inverted R-2R ladder.[1] Binary-weighted currents flow continuously in the shunt arms of the network; with 10V applied at the reference input, 0.5mA flows in the first, 0.25mA in the second, 0.125mA in the third, and so on. The I_{OUT_1} and I_{OUT_2} output busses are maintained at ground potential, either by operational-amplifier feedback, or by a direct connection to common.

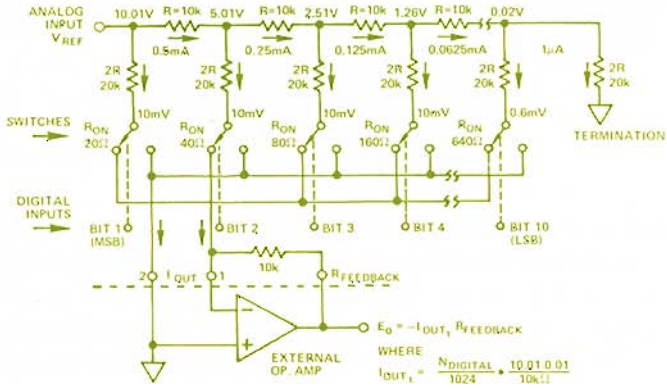


Figure 1. Functional diagram of the AD7520 D/A converter, with V_{REF} = 10.01V. Bits 5-9 are omitted for clarity.

The switches steer the current to the appropriate output lines in response to the individually-applied logic levels. For example, a "high" digital input to SW1 will cause the 0.5mA of the most-significant bit (MSB) to flow through I_{OUT_1}. When the digital input is "low," the current will flow through I_{OUT_2}. If I_{OUT_1} flows through the summing point of an operational amplifier and I_{OUT_2} flows to ground, then "high" logic will cause the nominal output voltage of the op amp to be - (0.5mA) x (10kΩ) = -5V, for a positive reference voltage of 10V, while "low" logic will make the contribution of Bit 1 zero. With all bits *on* (i.e., "high"), the nominal output will be -9.99V. With all bits *off*, the output will be zero.

Linearity errors, and – more important – their variation with temperature, are affected by variations of resistance in both the resistors and the switches. As we have seen, the resistor-network tracking is excellent. However, it is natural to expect that the switches, while tracking one another, will not track the resistance network. With identical switches having realistic resistance values (say 100Ω), one would expect that, as temperature changed, the variation of resistance in the series legs would transform the network into an R-*n*R network, with *n* sufficiently different from 2 to destroy the binary character of the network and cause the converter to become non-monotonic.

The key to the linearity of the AD7520 is that the geometries of the switches are tapered so as to obtain *on* resistances that are related in binary fashion, for the first 6 bits. Thus, the nominal values of switch resistance range from 20Ω for the first bit, 40Ω for the second bit, through 640Ω for the last 5 bits. The effect is, as can be seen in Figure 1, to provide equal voltages at the ends of the 6 most-significant arms of the ladder (0.5mA x 20Ω = 0.25mA x 40Ω, etc. = 10mV). Since this drop is, in effect, in series with the reference, it causes an initial 0.1% scale-factor ("gain") error, which is well within the specifications, but does not affect the linearity. Since the switches tend to track one another with temperature, linearity is essentially unaffected by temperature changes, and the gain error is held to within the 10ppm/°C specification.

Ten-bit linearity could, of course, have been obtained by scaling the *on* resistance of all the switches to a negligible value, say 10Ω, but the switches would have required very large geometries, which would result in a 30% to 50% larger chip, at a substantial increase in cost.

Figure 2 illustrates one of the 10 current switches and its associated internal drive circuitry. The geometries of the input devices 1 & 2 are scaled to provide a switching threshold of 1.4V, which permits the digital inputs to be compatible with TTL, DTL, and CMOS. The input stage drives two inverters (4, 5, 6, & 7), which in turn drive the N-channel output switches.

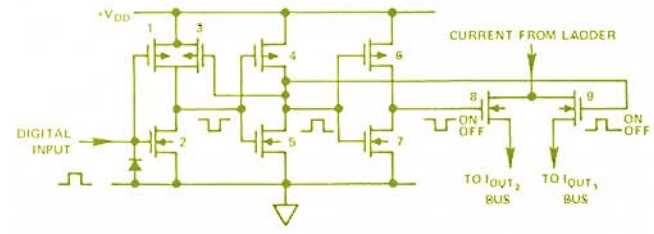


Figure 2. CMOS switch used in the AD7520. Digital input levels may be DTL, TTL, or CMOS.

EQUIVALENT CIRCUIT

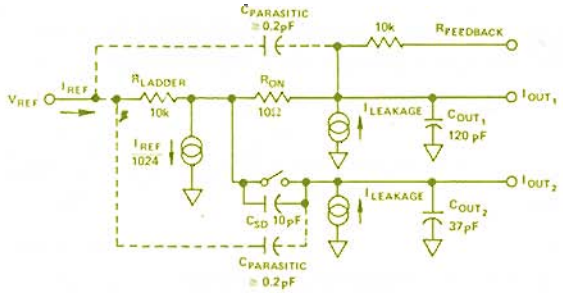
Figure 3 shows the equivalent circuit of the AD7520 at the two extremes of input, all inputs "high" (a) and all inputs "low" (b). V_{REF} (or I_{REF}, if a current reference is used) sees a nominal 10kΩ resistance, regardless of the switch states. The current source $I_{REF}/1024$, represents a 1 LSB current loss through the 20kΩ ladder-termination resistor, shown in Figure 1. R_{ON}, in this case, is the equivalent resistance of all ten switches connected to the I_{OUT_1} bus (a) or the I_{OUT_2} bus (b). Current-source I_{lkg} represents junction- and surface-leakage to the substrate. Capacitors C_{OUT_1} and C_{OUT_2} are the output capacities-to-ground for the *on* and *off* switches. CSD is the open-switch capacitance.

The 1000:1 ratio between R_{ladder} and R_{ON} provides a number of benefits, all related to the small voltage drop across R_{ON}:

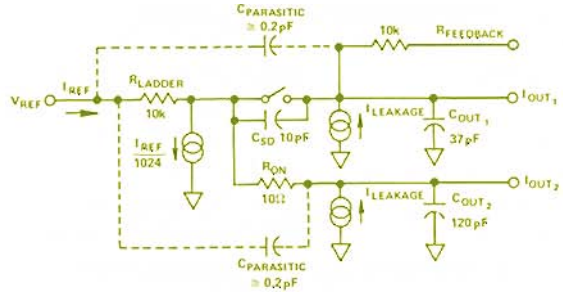
- V_{REF} can assume values exceeding the absolute-maximum CMOS rating, V_{DD}. For example, V_{REF} could be as large as ±25V, even if the AD7520's V_{DD} rating were only +17V.
- The nonlinearity temperature-coefficient depends primarily on how well the ladder resistances track. Since R_{ON} is only a small fraction of R_{ladder}, any R_{ON} tracking errors will be felt only as 2nd- and 3rd-order effects.
- The same argument holds true for power-supply variations. Any change of switch *on* resistance, as the power supply changes, will be swamped by the 1000:1 attenuation factor. Power-supply rejection is better than 1/3 LSB per volt.
- If V_{REF} is a fast ac signal, the feedthrough coupling via CSD, the open-switch capacitance, will be negligible, again be-

[1] The inverted R-2R ladder is one of the structures shown (Figure 18, page II-38) in the *Analog-Digital Conversion Handbook*, edited by D. H. Sheingold, published by Analog Devices, Inc., 1972, 402 pp., $3.95. To order a copy on approval, initial the reply card and request L2.

cause of the 1000:1 voltage stepdown. The parasitic capacitances from V_{REF} to I_{OUT_1} and I_{OUT_2} comprise the major source of ac feedthrough. Careful board layout by the user can result in less than ½ LSB of ac feedthrough at 100kHz.



a. All digital inputs high



b. All digital inputs low

Figure 3. Equivalent circuits of the AD7520 D/A converter

Since the *on* resistance depends only on the value of V_{DD}, not the current through the switch, and the resistance network is unaffected by V_{REF}, the full-scale output current (all bits "high") is nominally $V_{REF}/10.01k\Omega$, less the "constant" current losses shown in Figure 3. This means that I_{OUT} is almost perfectly proportional to V_{REF} over the whole range from -10V to +10V. Equally important, the conversion linearity error (0.05%) is independent of the sign or magnitude of V_{REF}.

The extremely-low analog-linearity error at constant digital input results in excellent fidelity to the input waveform, which suggests some interesting possibilities for the AD7520 in the calibration and control of gain in signal generators, high-fidelity amplifiers, and response-testing systems.

APPLYING THE AD7520

The two most common forms of application are in unipolar D/A conversion (2-quadrant multiplication) and bipolar offset-binary conversion (4-quadrant multiplication), shown in Figures 4 and 5. Where high speed is not desired, the output amplifier may be an AD741. For faster response, the AD518, AD505, or AD509* may be used, with appropriate compensation and a 10–20pF feedback capacitor.

Unipolar conversion. The response equation for Figure 4 is nominally

$$E_o = -\frac{N_{binary}}{1024} V_{REF}$$

Responses to typical codes are tabulated. Since V_{REF} may be positive or negative, two-quadrant multiplication is inherent. Circuit gain is easily trimmed by adjusting V_{REF}, inserting adjustable resistance in series with V_{REF} or $R_{feedback}$, or by tweaking scale factors elsewhere in the system. As noted elsewhere, once set, using low-TC trim resistors, gain stability with temperature is excellent.

*For data on these amplifier types, request **L3**.

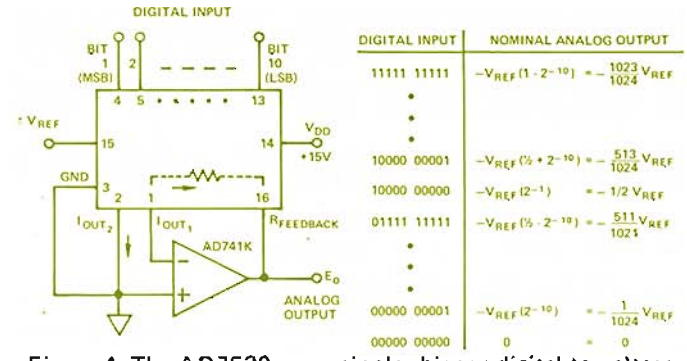


Figure 4. The AD7520 as a unipolar binary digital to voltage converter (2-quadrant multiplier)

Bipolar conversion. The offset binary response equation for Figure 5 is nominally

$$E_o = -\left[\frac{N_{binary}}{512} - 1\right] V_{REF}$$

Responses to typical codes are tabulated. If the MSB is complemented, the conversion relationship will be recognized as appropriate for a 2's-complement input, but with a negative scale factor. The MSB determines the sign, and the last 9 bits determine the magnitude in 2's complement notation. Since V_{REF} may be either positive or negative, 4-quadrant multiplication is inherent.

In this configuration, I_{OUT_2}, which is the complement of I_{OUT_1}, is inverted and added to I_{OUT_1}, halving the resolution (of each polarity) and doubling the gain. The 10MΩ resistor corrects for a 1/1024 difference (inherent in this technique) between I_{OUT_1} and I_{OUT_2} at zero (10000 00000). A2 is shown as a current inverter, but it might also be a voltage inverter, if the AD505 is used.

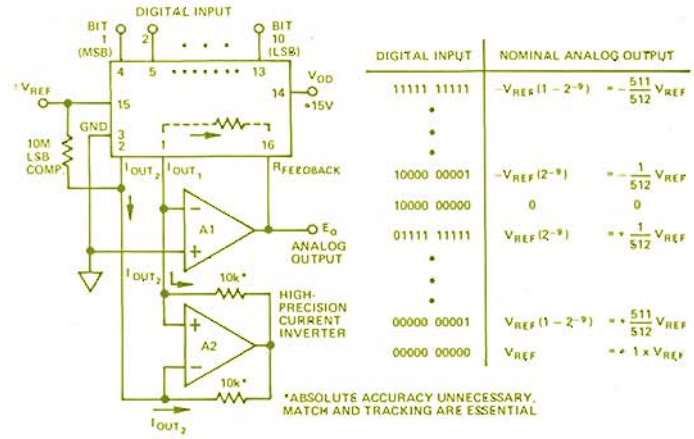


Figure 5. The AD7520 as a bipolar offset-binary digital-to-voltage converter (4-quadrant multiplier)

If sign-magnitude coding is desired, to obtain bipolar conversion with the full 10-bit-plus sign resolution, the output of the *unipolar conversion* circuit may be fed into a sign-magnitude converter, such as Figure 6. An AD7510 quad switch (see page 17) will handle two such circuits.

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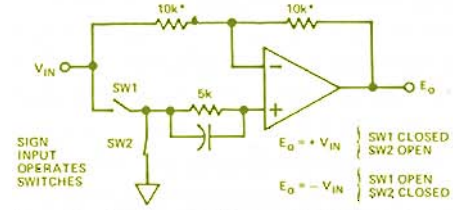


Figure 6. Sign-magnitude to bipolar converter.

HIGH-PRECISION THIN-FILM RESISTANCE NETWORKS
A USEFUL AND IMPORTANT TECHNOLOGY FOR THE CIRCUIT, INSTRUMENT, APPARATUS, AND SYSTEMS DESIGNER

by Lavar Clegg

High-precision thin-film resistor networks make it possible to design high-performance function circuits employing operational amplifiers and/or switches. Examples include sum-and-difference circuits, D/A converters, precision attenuators, and diode function-generators. At Analog Devices' Resistor Products Division*, the manufacture of standard and made-to-order networks at reasonable cost is a high art. In this article, we will discuss the nature of these networks, their properties, the materials and processes used in their manufacture, and the kind of design information that the circuit designer must consider to specify such networks for best results.

WHAT ARE THEY?

Resistance networks have come into increasing use as their cost comes down and their properties are better understood. There are two classes of resistor networks on the market:

a. The well-known low-cost networks that replace discrete resistors at savings in space, labor, and overall cost; they are now being sold in very large volume.

b. The less well-known thin-film high-precision networks that, besides providing savings in space and cost over assemblies of precision resistors, also provide the benefits of isothermal tracking, low capacitance and inductance, and improved reliability for critical applications.

The networks to be discussed here are of the latter class. They are characterized by high accuracy, high stability, low resistance-temperature coefficient (TCR), low noise, high reliability, low voltage-coefficient, and high speed.

THE NETWORK AS A COMPONENT

These important qualities of the network are most relevant when the precision resistance network is used as such, rather than as a group of independently-functioning resistors. In this sense, if the network is performing a function that depends on the location of all the resistors on a single substrate, with values that track, and with nearly-identical intrinsic properties, it can be considered as a circuit component, with properties specified in terms of its overall behavior. A general set of specifications that a typical network can be made to meet is listed in Table 1.

WHERE THEY ARE USED

Precision networks are likely to be found wherever attenuation, summing, division of voltage or current, setting of gains and ratios takes place. Perhaps the highest volume of usage of precision networks today is in ladder (or "bit weighting") networks for A/D and D/A converters. Examples of 12-bit ladder networks, which require tracking to better than 0.01%, include the AD850 modified-binary, and the AD855 R-2R.*

*For further information on the capabilities of ADI/RPD, use the reply card. Request **L4**.

TABLE 1. Properties of typical thin-film precision resistance networks.

Substrate size	0.050 to 3.5in (1.27 to 89mm)
Resistance values	10Ω to 10MΩ
Resistivity	50 to 500Ω/square
Resistance tolerance (absolute)	±0.001% to ±20%
Temperature coefficient (TCR)	±20 to ±100ppm/°C
TCR tracking	1ppm/°C
Noise	−50dB per MIL-STD-202, Method 308
Voltage coefficient	Below measurable levels
Operating temperature range	−65°C to 150°C
Power dissipation	to 60W/in^2 (9.3W/cm^2)
Resistance density	10^8Ω/in^2 maximum (15.5MΩ/cm^2)
Long-term drift, absolute	0.02%/1000h @125°C
Long-term drift, ratio	0.001%/1000h @125°C

Feedback and summing networks for amplifier circuits are a popular application. Figure 1 shows an example of such a network. Notice that complete symmetry exists between the two sides of this differential network, in order to optimize balance and minimize common-mode errors. Other applications are in voltage regulators and voltage dividers. Precision function fitters,[1] employing op amps, diodes, and resistance networks, become more practical in this day of precision resistance networks and infra-low-cost op amps.

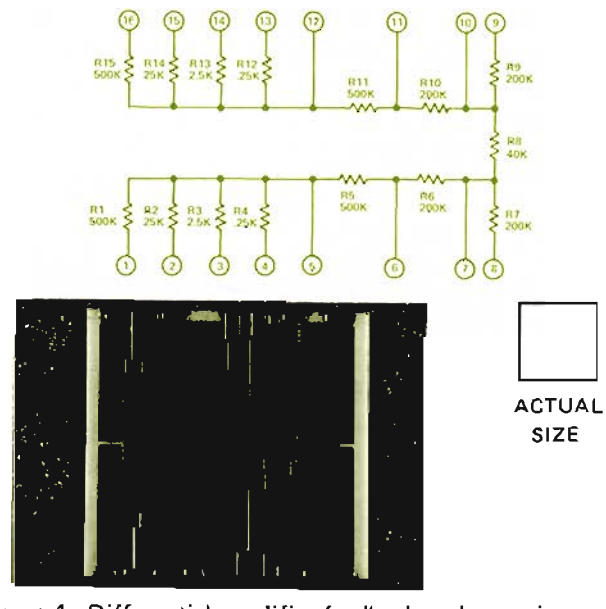


Figure 1. Differential-amplifier feedback and summing network. Actual size .4 x .4 inch. (10.2 x 10.2mm)

*For data on the AD850 and the AD855, request **L5**.

[1] See for example pp. 52-55 and 94-97 in *Nonlinear Circuits Handbook*, edited by D. H. Sheingold, published by Analog Devices, Inc., 1974, 534pp., $5.95. To order a copy on approval, initial the reply card and request

Applications for these networks occur in every conceivable discipline, including space, military, industrial, consumer, communications, instrumentation, biomedical electronics, and computer technology. The networks are of especial interest for systems exposed to the rigors of man and nature, such as the extremes of temperature, pressure, moisture, corrosion, vibration, and acceleration.

HOW THEY ARE MADE

1. MATERIALS

A thin-film circuit consists of a substrate, a layer of resistive material, and a layer of a conductive material, suitably etched into a pattern of resistors and interconnections. Its cross-section (not to scale) is shown in Figure 2.

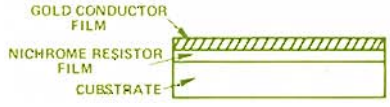


Figure 2. Cross section (not to scale)

Substrate. The most widely-used substrate material is alumina ceramic. It is the best compromise, given the choice among glass, silicon, and alumina. The ideal substrate would be perfectly smooth, flat, hard, non-porous, high in thermal conductivity, low in dielectric constant, durable, stable, and easy to "dice." No material rates high in all these conflicting properties. Glass is flat and smooth, with surface roughness of about 1μin (254Å); it is easily diced and has generally good electrical properties. However, it is susceptible to scratching, is generally fragile, and has very low thermal conductivity, a shortcoming serious enough to eliminate glass as an acceptable substrate for most precision networks. The passivated silicon wafer, while having excellent surface properties and high thermal conductivity, has excessive capacitive coupling because of the thin oxide layer and conductive bulk.

Alumina is durable, hard, reasonably flat, and is almost as thermally-conductive as silicon. Its major disadvantage, surface roughness (about 10μin, or 2500Å) can be overcome by glazing the top surface with about 2 mils (50μm) of glass. Alumina is also available in "fine-finish" form, with about 1/3 the surface roughness of ordinary alumina; not being polished, its cost is reasonable. Though other types of substrate exist, they are not usually used, either because of high cost or for technical reasons.

The most-commonly-used substrates are, therefore, glazed alumina, fine-finish alumina, or regular alumina (depending on the application), in thicknesses from 10-25 mils (0.25-0.64mm).

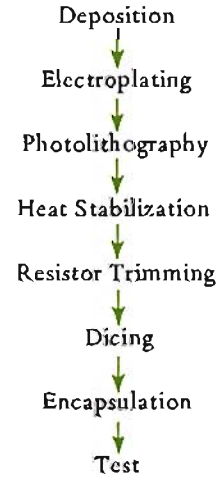
Thin-film resistors. The most widely-used materials are nichrome, tantalum, and various cermets. Our choice for precision networks is nichrome. It has a convenient range of sheet resistivities, does not require anodization, has a well-behaved TCR, and is inherently stable.

Conductor. Gold is used as the conducting film. Nearly ideal, it has low resistivity, low contact resistance, and good adhesion to the underlayer; it does not corrode or oxidize. It is suitable for all commonly-used interconnecting techniques: gold thermocompression bonding, aluminum- or gold-ultrasonic wire-bonding, and soldering. Aluminum is a viable alternative; it may be used more widely in the future if gold is priced out of the market.

2. PROCESSING

Table 2 is a flow diagram, outlining the major processing steps in simplified form. The actual process has many more steps with more-detailed designations and specialized purposes.

TABLE 2. Major Processing steps – Flow Diagram



Deposition. The thin films are deposited on the substrates in a specially-designed vacuum chamber by electron-beam evaporation. The evaporation parameters are carefully controlled for consistent and uniform films. Because dirt is the #1 enemy of thin-film processing, all deposition processes (including pre-deposition cleaning and preparation of raw substrates) are performed in clean-room areas, an important key to success. The capacity of this system is quite large: the $32ft^3$ ($0.91m^3$) chamber can process 20 3½" x 3½" (89 x 89mm) substrates, each of which may be fabricated into as many as 300 conventional-size resistor networks.

Electroplating. Only about 15μin (0.38μm) of gold are deposited in the vacuum chamber; greater thickness is built up by electroplating. To achieve good bonding properties and a conductor resistivity of less than 10mΩ/square, a nominal gold thickness of 150μin (3.8μm) is commonly used. The plating bath and plating processes are of course carefully controlled to provide a plating of the highest purity and uniformity.

Photolithography. The resistor-conductor pattern is created by selectively etching away portions of the originally-continuous films. Two complete photographic processes are required, one for the conductor pattern and one for the resistor pattern. In each, the surface is coated with light-sensitive photoresist, then exposed to light through a photomask, developed, and etched. To obtain acceptable and repeatable work from these processes with line-widths down to 1 mil (25μm) or less requires a highly-perfected and controlled process. Keys to success include control of the photoresist purity and thickness of application, precise exposure time, and controlled etching time.

Of course, no pattern can be of better quality than the photomask used; similar quality is required to those used in the semiconductor industry. Mylar is used instead of glass; while it has

the same high-resolution emulsion as glass and adequate dimensional stability, it has sufficient flexibility to conform to the ceramic substrate surface. (With glass masks, there would be areas of poor contact between surfaces, resulting in poor line definition in those areas.)

Heat stabilization. After photolithography and cleaning, the substrate is exposed to temperatures of 350° to 400°C in air for 1-2 hours. This bake serves two functions: it oxidizes the surface of the resistor film, providing a passivated layer of sorts, making the resistors less susceptible to mechanical and chemical attack than they would be without protection; and it renders the resistance stable in any heat-aging condition that may be imposed on the film at temperatures below the stabilization temperature. Because metal is used up by the oxidation, the process causes an increase in sheet resistivity of the film, typically about 75%. The exact duration and temperature of the bake is determined by the stability required, the initial and final resistivities, and certain properties of the film. Naturally, cleanliness and uniformity of temperature are essential to success, Figure 3 shows a typical substrate at this stage of the process.

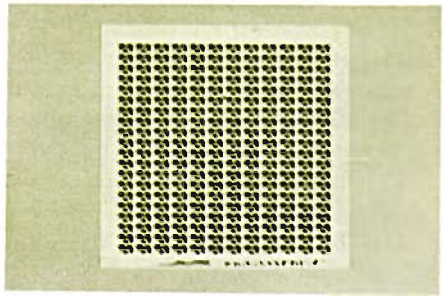


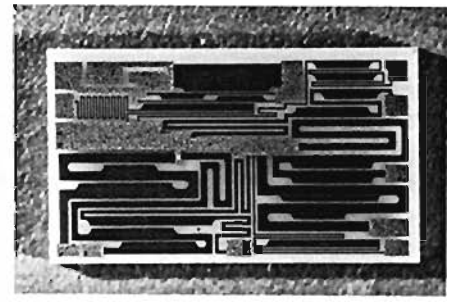
Figure 3. 3½" x 3½" (89 x 89mm) substrate with 240 resistor networks ready for trimming and/or dicing.

Trimming. Though trimming may occur either before or after dicing, the trend towards more automation and batch processing results in more trimming at the whole-substrate level. Since the resistance value of a resistor is determined by its shape, not its size, trimming involves changing the geometry of the resistor by cutting part of it away, under control. Cutting increases its resistance value. The method that is evolving towards universal application is laser-trimming, a clean, convenient operation that is compatible with (and conducive towards) automation, hence lower cost. Besides being fast, the laser is effective on all types of substrates.

Mechanical scribing, using a diamond stylus, is effective only on glass- or glazed-substrates. Though it has a number of limitations, including low speed, it can be quite accurately controlled and has a removal path width of about 0.2 mils (5μm), about 20% of that for a laser.

Dicing. The individual circuits are separated by sawing with a diamond wheel while the substrate is mounted on a holder with a temporary adhesive. The dice are then demounted and cleaned. A die resulting from this process is shown in Figure 4. An alternate process is to scribe the substrate with a diamond, then break, as is done with glass and silicon substrates. But alumina is quite hard, and tends to limit the diamond's life to just a few passes.

More practical is laser-score-and-break, using a laser with considerably more power than that used for trimming. After the substrate is scored to approximately 1/3 of its thickness, it is a simple matter to break it along the score lines. With quality close to that produced by sawing, but potentially lower cost (because the method is easily automated), this technique is growing in popularity.



ACTUAL SIZE

Figure 4. Single network after dicing. Actual size is .140 x .240 inches (3.6 x 6.1mm).

Packaging. The simplest package is no-package-at-all. The networks are shipped to the user after dicing and incorporated directly into hybrid circuits. Users do not require a great deal of micro-circuit equipment to benefit by the use of dice; as a result, this form of use is gaining in popularity.

However, for most uses, means of protection and interconnection are necessary. This requirement is satisfied by the same techniques and materials that are used throughout the integrated-circuit industry. Typical packages are multi-lead flatpacks, dual in-line, or round can with ceramic or glass seals. The resistor-network die is mounted and secured into the cavity of the package with epoxy, which is strong, stable, and thermally conductive. If an all-metal system is required, the back of the substrate will have been metallized, allowing the die to be soldered into the cavity.

Connections from the die to the package leads are made by aluminum ultrasonic wire-bonding, or by gold-wire thermo-

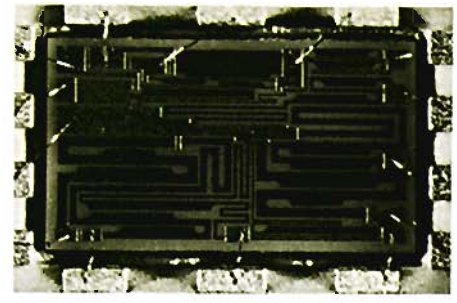
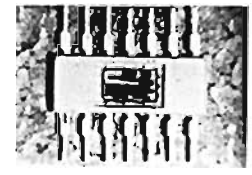


Figure 5. Cavity of TO116 header with resistor network mounted and wire-bonded.



ACTUAL SIZE

Figure 6. Network ready to be sealed.

compression bonding, using wire of 1 or 2-mil (25–50μm) diameter. Both allowable resistance and assembly considerations affect the choice of wire. Figure 5 and 6 show the die of Figure 4 mounted and wired. Figure 7 shows gold and aluminum wires on a single network.

The interconnections completed, the package is then hermetically sealed, either by welding or by soldering. The same machine is used to perform either operation, with the package relatively cold (i.e., below solder-melting temperature), while the seal frame and cover are heated sufficiently to flow-solder or weld the two surfaces. If hermeticity is not required, it is practical to pot the cavity with high-grade silicone resin. This method has been demonstrated to perform, over the extremes of temperature, as reliably as hermetic sealing. Hermetically sealed or otherwise, packages ranging in size from ¼" to 2" (6.4mm to 51mm) are available.

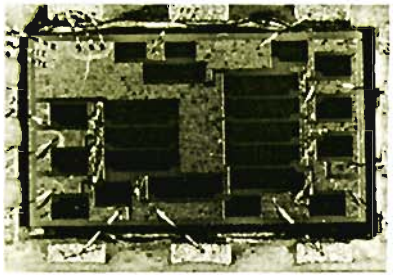


Figure 7. Example of large multiple wire bonds used in critical lead connection to decrease lead resistance. TO116 cavity.

CONTROLS

Because of the critical nature of the work and the large number of military applications in the early days of the industry, quality control is thorough and pervasive. A typical production flow chart will show that almost every single operation is followed by an inspection (mostly on a 100% basis) by a Q.C. function that is independent of Manufacturing. Visual inspections are performed with high-quality metallurgical microscopes at 50x to 100x. Additional inspections, performed on every lot of material, include: film-adhesion test, TCR check, gold-thickness measurement, wire-bond-strength test, hermeticity (leak) tests, dimensional inspections. All incoming raw materials are subjected to inspection and lot control. Manufacturing records are kept by lot, and these documents are subject to quality review before completed resistor networks are shipped to the customer.

SPECIFYING RESISTANCE NETWORKS

The most important thing to remember when specifying a network is that it is itself a component and should be specified in terms of the *overall performance of its function*, rather than the properties of its individual resistors. For example, a resistance-ladder network for a 12-bit D/A converter may be specified for accuracy, linearity, and monotonicity of its voltage (current) output in a particular conversion circuit. Its input and output impedance might also be specified. But none of these parameters requires direct specification (or measurement) of the tolerance of each resistor in the network.

This rule applies even to simple networks. For example, in a simple voltage divider with 2 resistors, depending on the interpretation, a specification of 0.01% can mean 3 different things (with a range of 5.3:1): resistance-ratio error, voltage-ratio error (% of ratio), voltage-ratio error (% of full-scale).

For high-accuracy applications, the method of application affects the means of specifying and testing, especially if low resistance values (usually less than 1kΩ) are involved, since their tolerance might be comparable to the resistance of the internal wire bond and the I.C. package lead. It is important to provide complete information on the use of the network and to define accuracy.

It is also important to specify which leads carry current, and which are to be connected to high-impedance amplifier inputs. The effects of temperature on accuracy may be specified either in terms of a range of resistance variation corresponding to a range of temperature variation, or by specifying 25°C accuracy plus TCR tracking (ppm/°C).

Power and voltage ratings are often written improperly. Power rating is meaningful only as it relates to temperature, life, drift, and the operating environment, in terms of the *function* of the resistor network. The meaningful rating for a simple voltage divider, for example, is the maximum operating level of V_{IN}, and any short-term overvoltage requirements. It would not be meaningful to rate the resistors equally in power or voltage, since the only common parameter is current. If a constraint of equal power ratings for the resistors were imposed, it might well create a sacrifice in tracking accuracy. Here are some rules for obtaining good power ratings:

1. Specify the network as a functional component, rather than as individual resistors.
2. Do not use separate (conflicting) power and voltage ratings.
3. Define the ambient operating conditions.
4. Do not be constrained to round numbers. Film resistors may be designed for any rating from zero on up.

Other electrical specs that are often important (if relevant) include settling time, capacitance, stability, noise.

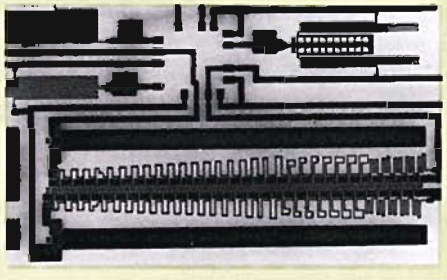
Also specify mechanical and packaging requirements. The package and lead configurations normally specified are those common in the I.C. industry, including TO-5, TO-8, TO-116 configurations, and metal, plastic, glass, and ceramic materials.

Environmental requirements must be specified as called for. Those characterized by MIL-STD-883 are commonly used and understood.

▶▶▶

EXAMPLE OF A NOVEL APPLICATION

Two resistors, equal in value, are designed for simultaneous active trim with a single trim pass. Each resistor increases by precise 5% increments to as high as 4.5x the initial value when all 31 steps are used. In addition, each resistor is trimmable linearly and separately up to 50% of initial value. This unencapsulated resistor network, which is used as a hybrid component, is completely compatible with automatic trimming techniques. Actual length of the resistors is 0.3" (7.6mm).



HIGH SPEED OP AMPS REVISITED – 1

WHAT DOES "HIGH SPEED" MEAN TO THE USER?

by Jerry Fishman

Because of the demand for increased speed in computers and data-acquisition systems, the circuit engineer is designing with higher-speed analog components than he may have used in the past. And nowadays, there is a much wider choice available to him, in the form of both IC's and discrete modules, each specified in terms of whatever its strong points happen to be, i.e., slewing rate, settling time, bandwidth, output current, stability, low noise.

Often the designer finds it difficult to interpret the manufacturers' specs in terms of his own application to make an informed choice. And when he uses the device he has chosen in his circuit, he may find that its performance is quite different from what he expected (or was led to believe he could obtain). There is often a world of difference between manufacturers' test circuits and the hurly-burly world of real applications.

There is no doubt that high-speed amplifier terminology can be confusing. What is a high-speed amplifier to one designer might be a medium-speed amplifier to another. A high slewing-rate amplifier, a fast-settling amplifier, and a wide-bandwidth amplifier - all are fast, but in quite different ways. In these pages, we shall seek to dispel some of the confusion by providing practical definitions of the specifications, relating them to applications, and discussing some of the factors that affect the design of practical high-speed circuits.

Since the great majority of high-speed amplifiers considered for use now (and increasingly in the future) are integrated-circuit, this discussion will lay heavy emphasis on integrated circuits. As the table on page 11 shows,* "high-speed" op amps are characterized by small-signal unity-gain bandwidths of the order of 10MHz or more, slewing rates in excess of about 20V/μs, submicrosecond settling times to within 0.1%, and settling times of the order of 1 μs to within 0.01%.

SLEWING RATE

Slewing rate is the maximum available rate-of-change of output voltage. If an ideal step could be applied to the input of an op amp circuit, the output rate of change would be limited, principally by the speed with which capacitance can be charged by current ($dV/dt_{max} = I_{max}/C$), either at the output (maximum output current into the load capacitance) or at some point inside the amplifier.

Slewing rate is affected by the external "gain" connection of the feedback elements; it is affected by the value of external compensating capacitance; it is affected by whether the configuration is inverting or non-inverting; and it very likely differs between the leading edge and trailing edge of the waveform. It is also affected by the portion of the response over which the measurement is performed (typically from 10% to 90% of the difference between the initial and final values).

*Ed. note: The table on page 11 provides a comparison of the specifications of typical members of various high-speed op amp families, both I.C. and discrete-module.

There is little uniformity among manufacturers on how to measure slewing rate. The spec usually quoted is the one that makes the amplifier look best. However, it should be measured for both leading and trailing edge and specified for the worst case, usually unity-gain, non-inverting. However, while there is no one correct method or configuration, it is important that the manufacturer and the user agree on the same criteria.

Figure 1 is a simplified representation of an operational amplifier that shows how the slewing rate is internally affected by the current in the input stage and the compensation capacitor. In Figure 1, the current through each collector circuit is I, and both are furnished by a current source, 2I. In the linear (small input-difference) mode, the currents are I + ΔI and I – ΔI, where the ΔI's tend to be small. However, if the input signal becomes large enough to shut one of the input transistors off (which happens when the amplifier is desperately trying to follow a fast input, and can't make it, creating a large difference signal), the current through Q2 can range from 0 to 2I. Since the active load usually seeks to maintain its current at the static value I, the difference current, I or –I, flows through the input of the next stage.

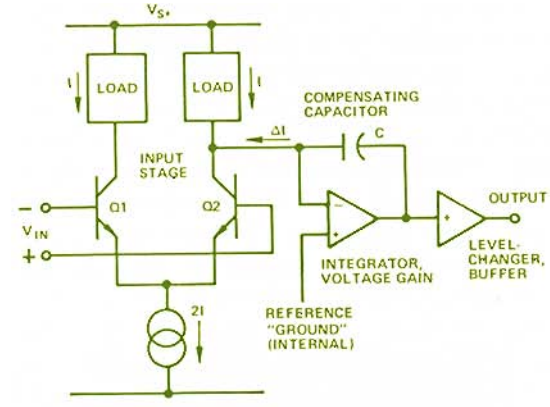


Figure 1. Simplified typical op amp configuration

The next stage is usually an integrator; that is, it has a constant 90° phase shift and an amplitude response that is inversely proportional to frequency (-6dB per octave). It controls the amplifier's overall frequency response; with the right value of capacitance, it will ensure stability over the whole range of resistive feedback ratios. (That is, a feedback amplifier must have a tailored response, rather than a "flat-out" wideband response, in order to be universally stable. More on this later.) With a constant current (I or –I) flowing through the capacitor, the output of the amplifier changes at the rate I/C; it cannot change at a faster rate. This is the internally-determined slewing rate. In the AD518, for example, the value of I

Portions of this article originally appeared in ELECTRONIC PRODUCTS MAGAZINE, November 19, 1973 issue, 645 Stewart Avenue, Garden City, N.Y. 11530, 1974 United Technical Publications, Inc., a Division of Cox Broadcasting Corporation.

is 400μA, and C = 5pF, which gives a nominal slewing rate of 80V/μs.

All operational amplifiers use compensation of this sort, but the actual circuitry can differ considerably. In some, the integrating capacitor is connected between the collectors; in others, it is "grounded," either to common, or to one side of the supply.* In many integrated-circuit op amps, it is connected externally, and chosen by the user for the best compromise between stability and bandwidth.

For a given value of signal gain, a non-inverting configuration may require more compensation than its inverting counterpart. Figure 2 shows two circuits that have gains of 1. But the non-inverting amplifier has a loop gain of A, while the inverting amplifier has a loop gain of A/2, which would lead one to expect that the non-inverting amplifier will require more compensating capacitance. Consequently, the inverting configuration will slew at a faster rate, if the user has connected a smaller value of compensating capacitance.

The relationship usually employed to relate slewing rate to full-power sinusoidal output is

$$dE_o/dt\big|_{max} = d(E_{oFS} \sin \omega t) / dt = E_{oFS}\,\omega$$

Since $\omega = 2\pi f$, the frequency for full-power output is

$$\frac{dE_o/dt\ _{max}}{2\pi E_{oFS}}$$

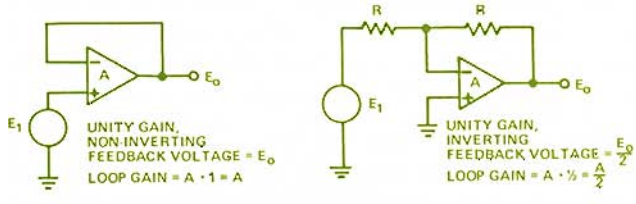


Figure 2. Inverting circuit has less loop gain

Thus, for a 10-volt amplifier, 6V/μs of slewing rate corresponds to a full-power frequency of 100kHz.

The usefulness of slewing rate as a measure of performance is rather restricted: It provides an approximation of the frequency range at which distortion becomes excessive, it suggests the narrowest pulse-width that may be gotten through an amplifier with reasonable fidelity, and it provides a measure of the sharpness of signals that may be applied with response predicted by the small-signal response. However, to predict the rate at which high accuracy can be maintained, one must know the *settling time.*

SETTLING TIME

Settling time† is the time elapsed from the application of an ideal step-input to the time the closed-loop amplifier output enters and remains within a specified error band, usually symmetrical about the final value (Figure 3). Settling time includes a brief propagation delay, the time required for the output to slew to the vicinity of the final value, the recovery from the overload condition associated with slewing (that capacitors must be discharged, and any thermal unbalances must be resolved), and the final time to settle to within the specified range.

continued on page 12

*741-type amplifiers are an example of this connection. For such amplifiers, the negative supply must be extremely well-regulated, since high-frequency noise and ripple are transmitted directly to the amplifier output.

†A comprehensive and useful discussion of settling time may be found in *Analog Dialogue*, Volume 4, No. 1

CHOOSING A HIGH-SPEED OP AMP

The general rule for packaged circuits applies: Pick the lowest-cost I.C. that you are sure will do the job; if you can't find (or adapt) one that will, it will become necessary to pick the most suitable discrete design.

It is usually the case that I.C.'s have considerable advantages in cost and size. However, to meet the needs of extreme performance requirements, modules may still be necessary. Examples of situations that require modules are:

- **Large amounts of power are involved — 20 to 100mA of output current at ±10V (the faster the circuit, the lower the impedances, hence the greater the power and dissipation requirements).**
- **Noise must be extremely low: less than 10μV rms (in a 5MHz bandwidth).**
- **Settling times must be less than 500ns to within 0.01% or 100ns to within 0.1%; slewing rates must be in excess of 120V/μs; and/or unity gain bandwidths must be greater than 35MHz; any or all of these on a min-max basis.**
- **Any or all of the above with internal compensation.**

Generally, a manufacturer's sales and applications engineers can be of assistance in making a good choice; the broader the product line available, the more reliable and dispassionate the advice that will be obtained, especially if the manufacturer, like Analog Devices, offers a wide variety of both IC and discrete high-speed amplifiers. The table below lists a number of the types available from ADI, both IC and modular, as examples of the available specification mix.*

RELEVANT CHARACTERISTICS OF
TYPICAL HIGH-SPEED OPERATIONAL AMPLIFIERS

at 25°C and V_s = ±15V, unless noted otherwise

Type Designation	Unity-gain BW (MHz) Typical	Slewing Rate (V/μs) Minimum	Settling Time (0.1%) Maximum	Settling Time (0.01%) Maximum	Price 1+ $U.S.
INTEGRATED CIRCUITS					
AD509S, differential	20	100	0.5	2.5	26.00
AD509K, differential	20	80	0.5	2.5	18.75
AD508J, differential	20	80	0.2(T)	1.0(T)	11.50
AD506J, inverting	4 to 10§	120	0.8(T)	2.0(T)	15.00
AD518J, differential	12	50	0.8(T)	2.0(T)	3.00
AD528J, differential FET	10	50	0.8(T)	—	18.00
AD507J, differential	35	20	0.9(T)	—	9.50
DISCRETE MODULES					
50J, differential FET	80	500	0.1	0.2(0.05%)	75.00
51A, differential FET	80	400(T)	0.14	0.35	99.00
48J, differential FET	15	125/90†	0.25(T)	0.3(T)	49.00
45J, differential FET	10	75	0.5(T)	1.0	37.00
44J, differential FET	10	75/50†	0.5(T)	1.0	42.00
120A, inverting	10 to 100§	250	—	1.0(T)	78.00
47A, differential FET	10	50	0.5(T)	1.0	77.00

§Bandwidth adjustable
(T) Typical value
† Inverting/non-inverting

*To request information on a specific type, use the blank spaces at the head of the reply card. For catalog information on the whole product line, request L7.

continued from page 11

This definition is now widely accepted. At one time, though, some manufacturers defined settling time in terms of the final "tail" only. When short settling times are quoted, the reader should make sure that the above "long-form" definition is the one used.

Settling time is a closed-loop parameter determined by a combination of amplifier characteristics, nonlinear as well as linear. Thus, it cannot be predicted readily from such open-loop specs as slewing rate and small-signal bandwidth. An extremely-high slewing rate does not insure a rapid settling time, because slewing rate is only one of the factors affecting it. An amplifier with an extremely-high slewing rate can often have a long settling time.

Normally, the final value achieved in the definition is not necessarily the exactly correct value of amplifier output, since that value is affected by amplifier open-loop gain, offset voltage and drift, and common-mode error. Settling time to within a given band cannot be defined at all if noise is excessive. However, a desire for a given level of settling-time performance usually implies that the amplifier must also have satisfactorily-small levels of error due to such causes.

For example, fast-settling amplifiers are used in many applications for high-accuracy conversion systems requiring fast settling to either 10- or 12-bit accuracy, within ±½ least-significant bit (0.05% or 0.0125%). If an amplifier has a rated output voltage of 10V, 0.0125% represents 1.25mV of error. For such high degrees of resolution, other errors, as well as settling time, must be minimized.

Op amps designed for optimum response at high closed-loop gains at moderate frequencies often have transfer functions that provide only marginal stability when the closed-loop gain is reduced to values near unity. The amplifier used for fast settling to high accuracy should have a closed-loop response that is (at least theoretically) only slightly less than critically damped, since any oscillation or ringing may prolong settling time.

And, in practical circuits that have stray capacitance, the added lags caused by the external loop elements will cause a system to ring, even if it has an amplifier with sufficient phase margin. For this reason, designers of fast-settling op amps try to have the open-loop frequency characteristics strongly dominated by a single time constant. This is stated in many ways, all with the same meaning: constant 90° phase shift, −6dB/octave (or −20dB/decade) rolloff, unit lag, exponential time response.

The term "settling time" is also used to indicate the time required to restore the output to its original level after it has been disturbed by a transient associated with a step change of load. In conversion circuits, the settling time is the time required to achieve and remain within ±½ least-significant bit of final value.

Because of the low final-value errors and wide-ranging slewing transients, settling time is quite difficult to measure. Measurement circuits for settling-time in analog circuits are described in Volume 4, No. 1 of *Analog Dialogue*; settling-time measurements for conversion circuits are shown in the *Analog-Digital Conversion Handbook*, starting on page II-116.

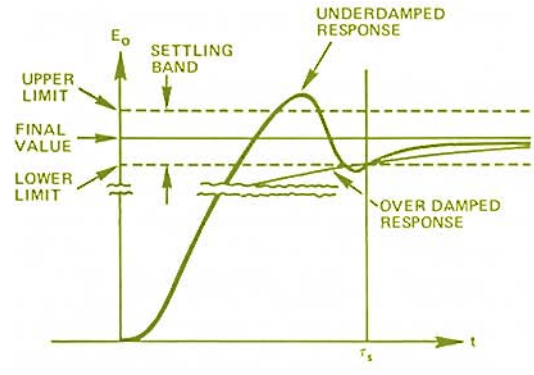


Figure 3. Examples of settling time. Voltage scale greatly magnified in vicinity of final value.

MINIMIZING SETTLING TIME

The settling time of a practical op amp circuit is determined by the input source, the operational amplifier, and the associated circuitry (including stray capacitances and the non-ideal nature of circuit components, such as resistors and diodes). While the amplifier alone is predictable, as specified in a certain configuration, what is painstakingly gained in amplifier design can be lost without careful circuit design. Some of the elements of good high-speed design are:

Power supplies and grounds should be properly connected and bypassed (typically, with 0.1μF ceramic capacitors, connected at the op amp socket) to avoid introduction of noise, stray feedback paths, or ground loops. Load- and summing-point-capacitances should be minimized or compensated for. All connections should be short and direct, to minimize lead inductance and capacitive coupling.

Resistors should be metal-film types; they have less capacitance and stray inductance than wirewound types, yet have excellent accuracies, temperature coefficients, and tracking.

Capacitors in critical locations should use extended-foil construction, with dielectrics of polystyrene, Teflon, or polycarbonate, to minimize dielectric absorption.

Circuit impedance levels should be as low as is consistent with the output capabilities of the amplifier and the signal source. Don't overlook sockets or the p.c. board itself as possible sources of dielectric absorption. Avoid pole-zero mismatches in any feedback networks used with the amplifier.

SLOW BUT ACCURATE

As noted, fast settling to an uncertain final value is useless. On the other hand, not-too-slow settling to an accurately determined final value can be quite useful. For example, the low-drift, high-gain, high CMR, low-noise (0.5μV/°C max, 106 & 110dB min, 0.6μVp-p max – 0.1 to 10Hz) AD504M* integrated-circuit op amp, connected for gain-of-100, settles to within 0.01% in about 1ms, quite adequate for chart recorders, panel meters, and many measurement circuits. ▶▶▶

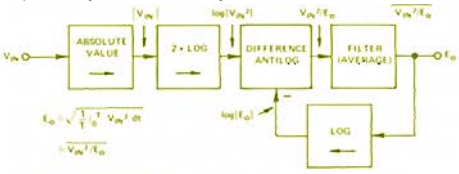
To be continued. The next installment will discuss stability and phase margin, and the use of Bodé plots as an indispensible tool for predicting small-signal instabilities.

*For information on the AD504 family, request L2.

LOW-COST RMS-MEASURING CIRCUIT

MODEL 440 HAS LESS THAN 2mV ±0.05% ERROR, COSTS $42. IN 100's

The Analog Devices Model 440* is a "true-rms" to dc converter designed for applications in instrumentation, measurement, and data acquisition, wherever stationary waveforms of unknown or arbitrary shape are encountered. The process of computing the root mean-square (rms) involves squaring the positive or negative input signal, averaging it to obtain the mean-square, and square-rooting to obtain the *root mean-square*. The Model 440 performs these operations in a feedback configuration, using logarithmic circuitry for squaring and rooting.



WHY RMS?

There are a number of solid reasons for measuring rms, rather than some other property of a waveform, based on its physical and mathematical properties.

The rms is a fundamental physical measurement: it is a measure of the heating value of a voltage or current applied to a resistor. Over the averaging interval, all waveforms having the same rms voltage or current will dissipate exactly the same amount of energy in the resistor, irrespective of the variation with time. This is true whether the waveform is constant (dc), sinusoidal, biased-ac, random, or a train of pulses.

The rms is a fundamental statistical parameter: for any stationary (unchanging general shape) zero-mean (e.g., ac-coupled) process, the rms is equal to the standard deviation of that process. Whether the distribution measured by the electrical waveform involves electrical random noise or the size of apples on a conveyor belt, the rms is a valid measure of the standard deviation, for large sample size.

The rms permits combination of uncorrelated quantities: If orthogonal or uncorrelated quantities are summed, the rms of their sum is equal to the square-root of the sum of the squares of their individual rms values.

*For information on the Model 440, request L8.

RMS vs. MAD (MEAN-ABSOLUTE DEVIATION)

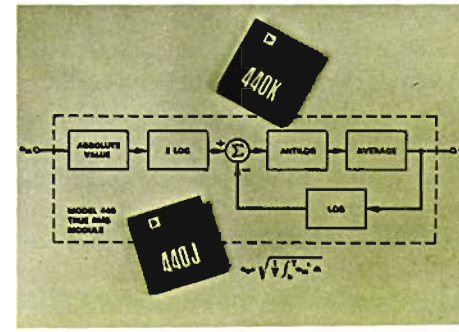
Low-cost rms meters (and, sadly, some expensive meters) have, in the past, been likely to read a calibrated version of the average of the absolute deviation (i.e., the full-wave rectified signal), rather than rms. Since the most popular ac waveform has been the sine-wave, the mad has been multiplied by 1.111 to read true rms. Unfortunately, this calibration constant can differ widely from waveform to waveform (see table); while it can be preset for known waveforms, this is out of the question for unknown or variable-duty-cycle waveforms, such as SCR's (silicon controlled-rectifier) and variable-width pulse trains.

TECHNIQUES

While many techniques are available to the computer-minded experimenter, the two in widest use are thermal converters and computing types using feedback, such as the 440. While the former have very wide bandwidth (at the high end) and are capable of excellent accuracy, they involve significant dissipations and temperature rise, cannot average slowly-varying waveforms very well, and may require op-amp buffers that will degrade performance. Computing types, on the other hand, are quite flexible; by the use of additional capacitance, for example, the 440 can accurately (1%) convert rms to dc over bands from 100kHz (-3dB @ 500kHz) down to 1Hz (10μF connected externally).

With offset drift of ±0.2mV/°C maximum and "accuracy" drift of ±0.02%/°C maximum, reasonable accuracy is maintained over the whole 0° to 70°C temperature range. Besides low cost, wide bandwidth, good accuracy, and flexibility, the 440 also boasts small size (1.5" x 1.5" x 0.41", 38x38x10.4mm) and light weight (40g). Available from stock, it's priced at $62 (1-9), 440J, and $75, 440K.

▶▶▶



RELATIONSHIPS BETWEEN RMS AND OTHER PARAMETERS OF SEVERAL COMMON WAVEFORMS

WAVEFORM	CREST FACTOR V_M/RMS	RMS/MAD
SINE WAVE	$\sqrt{2}$ 1.414	$\frac{\pi}{2\sqrt{2}}$ 1.111
SYMMETRICAL SQUARE WAVE	1	1.00
TRIANGULAR WAVE OR SAWTOOTH	$\sqrt{3}$ 1.732	$\frac{2}{\sqrt{3}}$ 1.155
GAUSSIAN NOISE (CREST FACTOR 1 2 3 4 5; 10^{-6} 10^{-3} 10^{0} PROBABILITY OF GREATER CREST FACTORS; EXAMPLE: C.F. > 4 HAS A PROBABILITY OF < 0.01%)		$\sqrt{\frac{\pi}{2}}$ 1.253
PULSE TRAIN	$\frac{1}{\sqrt{\eta}}$	$\frac{1}{\sqrt{\eta}}$
	η: 1, 1/4, 1/16, 1/64, 1/100 — C.F.: 1, 2, 4, 8, 10	1, 2, 4, 8, 10
SINE-SQUARED	$\sqrt{8/3}$ 1.633	1.225

LOW NOISE, NON-INVERTING CHOPPER OP AMP

Model 261* is a 2nd-generation non-inverting chopper amplifier designed to replace Analog's winning Model 260. The 261 has higher open-loop gain (10^7) and lower noise (1μVp-p *max*, 0.01–10Hz), and runs at a higher chopper frequency (3500Hz vs. 500Hz) to minimize chopper intermodulation and external noise-coupling problems. In addition, the shielding has been improved to eliminate intermodulation with chopper signals from adjacent amplifiers. The overall improvement includes such benefits as reduced distortion for 100Hz signals and freedom from chopper spikes.

In addition to its low noise, the 261's voltage drift is as low as 0.1μV/°C *max*, with 5pA/°C *max* offset-current drift (261K), and it has low initial offsets of ±25μV (adjustable to zero) and 300pA *max*.

Despite these improvements, size and cost (1-9) are the same for the 260, (1.5" x 1.5" x 0.62", 38x38x15.8mm), $49 for 261J and $64 for 261K.

WHY NON-INVERTING CHOPPERS?

Low-drift chopperless op amps have been considerably improved in recent years; examples include the 184 and 43K, and the I.C. AD504†. Yet, for high-gain applications, choppers still provide the lowest voltage drift and noise, combined with low bias current.

There are excellent inverting chopper-stabilized op amps available, such as the 234†. Though they are more versatile and have wider bandwidth, low input impedance makes their use impractical in preamplification of signals from high-impedance sources or unloading of potentiometers in precision measurement-circuits.

The 261 is especially well suited to dc and low-frequency measurements, with its bandwidth (–3dB) of 100Hz. Gain is adjusted by an external (non-loading) feedback divider, and input impedance is essentially $10^9\Omega$, for closed-loop gains up to 1,600. ▶▶▶

TWO IMPROVED FUNCTION MODULES

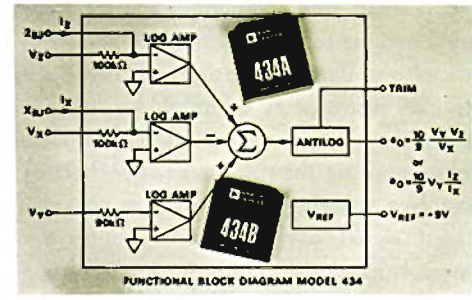
434 WIDE-RANGE MULTIPLIER/DIVIDER COMPUTES ZY/X WITH <0.25% ERROR

Model 434‡ has 3 inputs, which enable it to perform as

- a 3-variable multiplier-divider
- a multiplier with fixed, adjustable, or variable scale factor
- a divider with fixed, adjustable, or variable scale factor
- a squarer, rooter, geometric-mean, or root-sum-of-squares computer.

Not only does it have excellent overall accuracy, but in addition, the use of log-antilog circuitry gives it a wide dynamic range. Its output error, after adjustment, of 1mV ±0.15% of reading, means that output levels of 100mV will retain an error less than 1¼% of actual value, or *0.0125% of full scale!*

All inputs accept voltages from 0 to 10V; and the Z and X (ratio) inputs also accept current. This flexibility means that input currents may be applied directly from transducers (such as photodiodes). It also means that arbitrary values of input resistance may be used to allow the inputs to be scaled to any voltage levels.



For division and square-rooting, unlike inverted-multiplier circuits, the 434 will provide accuracy that is pretty much independent of denominator level, as long as the output is within the rated range.

Besides all these features, the 434 contains a reference source, which may be used as a constant scale factor for 2-variable operations, making it unnecessary to depend on external reference sources or the device power supply.

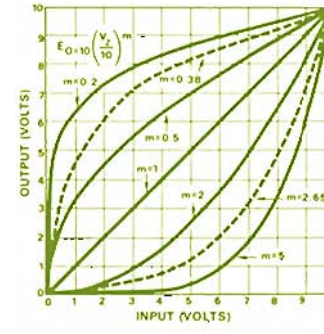
In size, it is a compact 1.5" x 1.5" x 0.62" (38x38x15.8mm). It is available from stock at $75 (434A) and $87 (434B) for (1-9). ▶▶▶

433B MULTIFUNCTION CIRCUIT: $Z(Y/X)^m$ PRODUCTS, QUOTIENTS, POWERS, ROOTS, RECIPROCALS

More flexible than the 434, more accurate than the 433J, the new 433B§ will perform all of the operations of the 434; but *in addition*, the connection of a pair of external resistors permits the ratio to be raised to a power (integral or fractional) from 0.2 to 5.0.

The 433B is useful for obtaining arbitrary powers and roots, which may be used in function-fitting and -generation, transducer linearization, ideal gas calculations, and in developing power-series approximations.

Like the 434, the 433B will operate over the –25°C to 85°C temperature range. Its 25mV (F.S.) error at 25°C is 1/2 that of the 433J; its 2mV offset is 1/2.5 that of the 433J. Its dimensions are the same: 1.5" x 1.5" x 0.62" (38x38x15.8mm),



availability is from stock, and price is $87 (1-9). ▶▶▶

*For complete information on the 261, request **L9**.

†For information on these amplifiers, request **L10**.

‡For information on the 434, request **L11**.

§For information on Models 433 (J & B), request **L12**.

TEMPERATURE MEASURING CIRCUIT BORROWS POWER AND REFERENCE FROM DPM

by Jim Hayes*

The AD2006† line-operated digital panel meter (DPM), introduced in *Analog Dialogue* 7-2, was designed with some interesting features that facilitate the design of measurement systems in which it might become involved. Two of its features make it especially ideal for the design of simple instruments:

1. It has dc power outputs of ±15V @ 10mA and ±5VDC @ 50mA. These dc power outputs allow the meter to power external circuitry associated with it, such as op amps or an instrumentation amplifier, without calling for an additional power supply. It is obvious that such an amplifier might be used to scale up small-amplitude inputs for measurement by the AD2006, in a small, self-contained measurement system.

2. The meter's reference voltage is available as the source of excitation for a transducer, generally via an amplifier stage that provides gain or attenuation (and power boost, in any event). The meter's reference-input terminal, normally used with its own reference voltage, can also be connected to an external reference source, for example, the excitation voltage for a bridge-type transducer. Either way, since the DPM's reading is proportional to the *ratio* of the input to the reference, it will be independent of variations of the reference with time, temperature, etc., to the degree that the transducer output is proportional to the reference voltage.

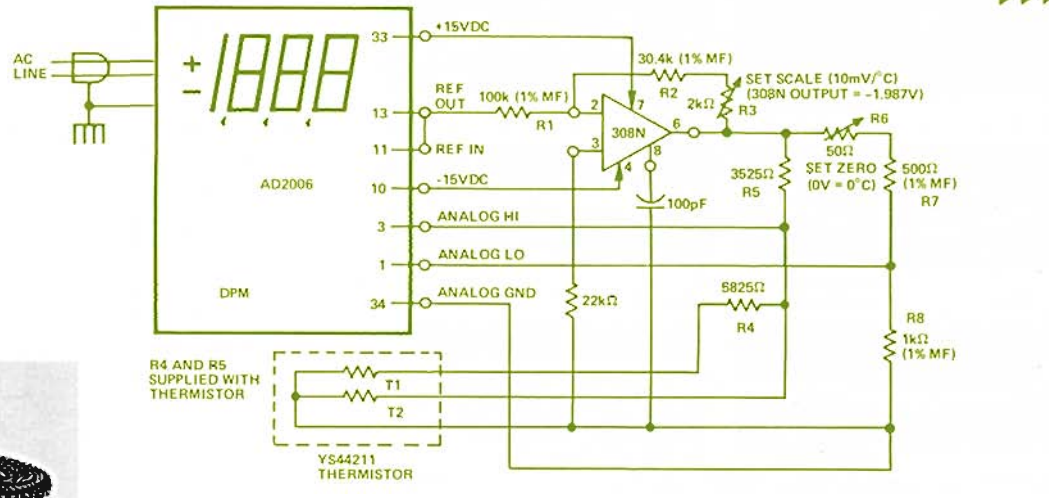
It is feasible, then, to build a complete measuring system, for some applications, making use of the DPM and just a few external components. The schematic diagram illustrates a practical *ad hoc* instrumentation application that works.

DIGITAL THERMOMETER

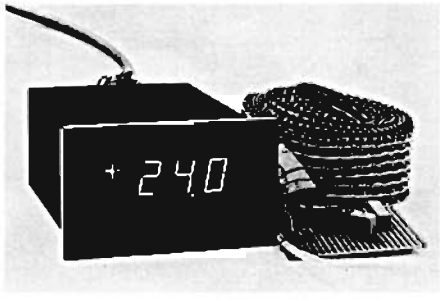
We needed an accurate temperature-measuring instrument for use in our engineering labs for testing new products. It was decided to use a thermistor in a bridge circuit, with the excitation voltage developed from the DPM's reference, and the output read differentially by the DPM.

The thermistor network chosen is a Yellow Springs YSI-44211. In order to supply a stable 2V of excitation, the internal reference output of the AD2006 was used, scaled and buffered by an AD308N op amp, to ensure that the loading of the reference would not greatly affect its stability. The AD308N is, of course, powered by the ±15V outputs of the AD2006. Trims were included for calibrating the circuit, so that the meter would read 00.0 at 0°C and 50.0 at +50°C (i.e., a 10mV/°C calibration). If calibration is desired in degrees Fahrenheit, the caption describes the necessary changes, in order to obtain 10mV/°F and 00.0 at 0°F.

The final result is a thermometer with a resolution of 0.1°C and accuracy error of ±1°C, typically reading temperatures in the range -55°C to +85°C to 1/10 of a degree. It has been in use in the laboratories at Analog Devices during the past year. Not only did it provide us with an accurate temperature-measurement tool and confirm the power-output and ratiometric aspects of the AD2006, but it has also given us another (albeit small) increment of life-testing history: one year, several such circuits built, no failures, many experiments expedited at low cost as a result of the circuit's usefulness.



Complete Electrical Thermometer Circuit. Readout is in °C. For readout in °F, R_2 = 54.9kΩ, R_3 is 5kΩ, R_6 is 100Ω, and R_7 is 1.05kΩ. For 10mV/°F scaling, set the AD308N output to 3.576V. Adjust R_6 for zero output at 0°F. The thermistor is manufactured by Yellow Springs Instrument Co., Yellow Springs, Ohio, 45387. It is available from many major distributors.



*Jim Hayes is Product Marketing Specialist for DPM's.
†For complete information on the AD2006, request **L13**.

REDUCING MULTIPLIER LINEARITY ERRORS

CROSS-FEED REDUCES 2nd HARMONIC DISTORTION AND FEEDTHROUGH

by Lewis Counts*

In many transconductance-multiplier designs, the "X" feedthrough error has a pronounced quadratic component. That is, for Y = 0 and X swept over the range ±10V, a crossplot (Figure 1) shows that the output, instead of being zero, is approximately equal to $(A + BX + CX^2)$. A is removed by the conventional offset adjustment and B is removed by the linear feedthrough (Y_O) adjustment, but the remaining term appears to be part of the irreducible nonlinearity of the device. It is one of the major manifestations of linearity error.

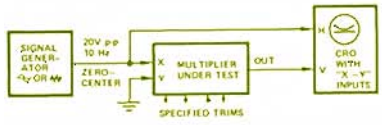


Figure 1. Multiplier "X" feedthrough crossplot test circuit. Horizontal setting: 2V/cm, dc-coupled, zero in center of screen. Vertical setting: 50mV/cm, dc-coupled zero on screen centerline.

The good news is that this feedthrough can be greatly reduced, by factors from 2 to 5, with some improvement to overall X linearity. The slightly-bad news is that it requires an additional "tweak." However, considering that low-cost multipliers, such as the 426, the AD530, and the AD532 can be helped in this manner, an overall cost saving is possible. Figure 2 is a set of "before and after" oscilloscope crossplots that show, rather dramatically, what can be achieved.

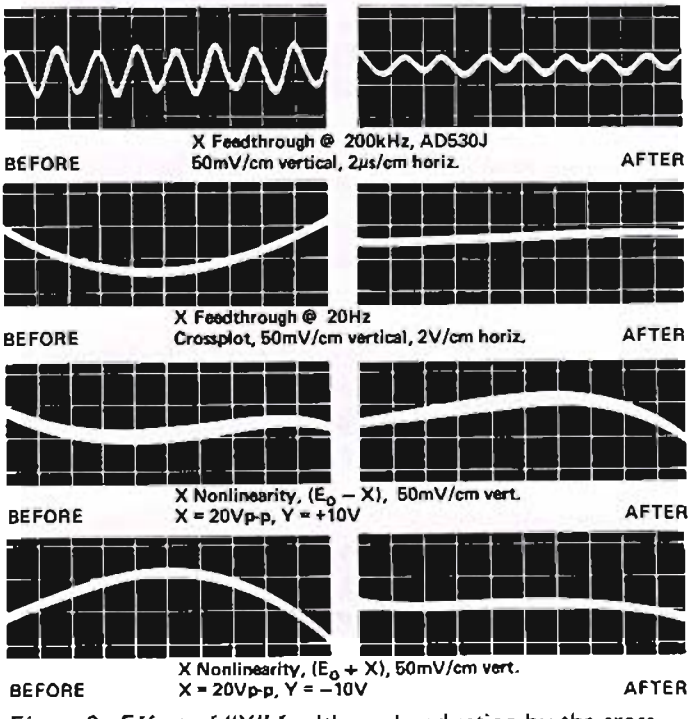


Figure 2. Effect of "X" feedthrough reduction by the cross-feed technique with a typical IC multiplier: AD530J

The "cross-coupling" compensation technique is described rather fully in the *Nonlinear Circuits Handbook* (see p. 19). It will be summarized briefly here. It is evident that the parabolic waveshape with Y = 0 indicates that a small fraction of X, (CX), is, in effect, being coupled into the Y portion of the circuit, resulting in a CX^2 term at the output. The solution, therefore, is to externally feed a small fraction of X (C'X), with opposite polarity, into the Y input, to cancel the internally-coupled increment. This is done, in practice, by first determining from the scope picture what the polarity of the error is (a "smile" is positive, a "frown" is negative). If the error is positive, a small fraction of X is fed into the negative Y input (labeled –Y) or resistively summed into the Y-offset terminal (Y_O or Y_R). If the error is negative, a small fraction of X is summed with Y passively, and the gain is retrimmed to compensate for the slight attenuation of Y. In either case, the X increment is adjusted until the parabolic shape is cancelled.

All normal trims should have been adjusted before this linearization adjustment is performed. The input signals should be at low impedance, and usually are, if they're from op amp outputs. The scheme works for parabolic, but not 3rd order nonlinearity. It can theoretically also be used for Y, but returns are diminishing. Trim circuits for several susceptible ADI multipliers† are shown in Figure 3.

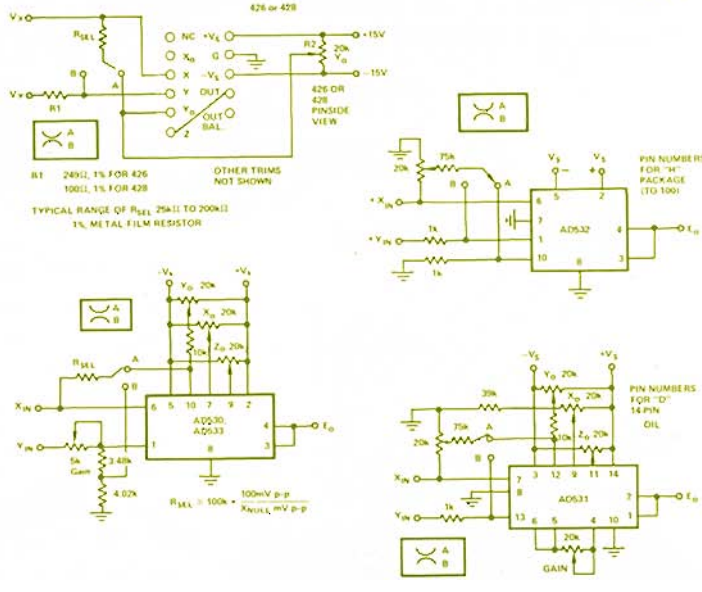


Figure 3. Linearizing circuits for Analog Devices multipliers. "A" connections are to correct for positive feedthrough error. "B" connections correct for negative error.

*Lewis Counts is Manager of Analog-Module Engineering at ADI's Modular Instrumentation Division and the author of chapters on multipliers, dividers, and rms circuits in the *Nonlinear Circuits Handbook*.

†For technical data on these multipliers, request **L14**.

USING CMOS SWITCHES FOR.....

by Jerry Whitmore

LOW-COST SAMPLE-HOLD

The sample-hold circuit shown in Figure 1 uses an AD7510K quad analog CMOS switch, two IC op amps (AD301A and AD741K), and a handful of miscellaneous components.* The circuit consists of a capacitor-to-ground, unloaded by a unity-gain follower (A2), in a feedback loop. During *sample*, the output of the follower is fed back to the negative input of op amp A1, while the signal is applied to the + input. The output of A1 must do whatever it can to force the voltage on C2 (hence the output) to track the input. During *hold*, the loop is opened, and the charge remains on the capacitor (except for leakage).

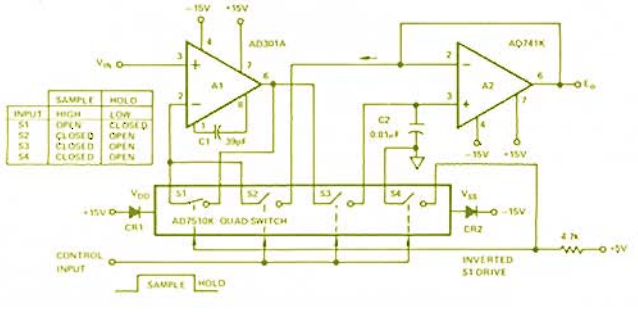


Figure 1. Schematic diagram of sample-hold circuit. Parts cost (purchased in 100's) is less than $16.

Switching is performed by an AD7510 quad switch. S4 inverts the logic applied to S1; it is closed when S2 & S3 are open (*hold*), and open when they are closed (*sample*). In *hold*, S1 connects A1 as a follower, S2 disconnects A1's –input from the output of A2, and S3 disconnects A1's output from the capacitor. In *sample*, S1 opens the local loop around A1, S2 connects the output of A2 to the –input of A1, and S3 connects the output of A1 to C2 (+ input of A2).

In *hold*, the leakage rate, $dV/dt = I_{LKG}/C$, is dominated by the op amp's bias current, 75nA, and is about 7.5mV/ms. This means that for 8-bit accuracy (½LSB = 0.2%FS ≅ 20mV), a signal could be held for more than 2.5ms without excessive degradation. For conversion rates of 5-10kHz, the total signal degradation due to this droop would only be about 0.02%FS.

Dynamic error (*sample* to *hold*) is determined by the switch *aperture time* (~700ns) and the maximum rate-of-change of the signal (Figure 2). For sine waves with full 20Vp-p amplitude, aperture errors are less than ½LSB of 8 bits for frequencies up to 300Hz, and proportionally less for lower-level inputs (slower changes).

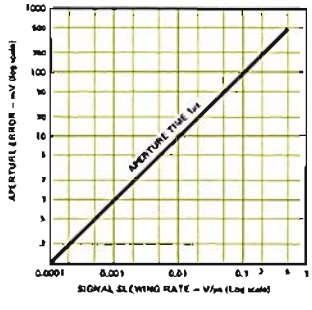


Figure 2. Aperture error as a function of input-signal slewing rate (within response capability of the system).

*For information on the quad switch and op amps, request **L15**. For information on complete sample-holds manufactured by Analog Devices, request **L20**.

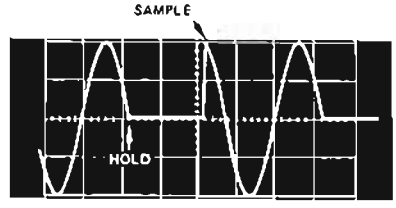


Figure 3. Typical waveforms of sample-hold circuit. Sinewave input is 20Vp-p, 2kHz. Vertical scale is 5V/division; horizontal scale is 200µs/division. Hold-to-sample is slew-rate limited.

During *sample*, small-signal bandwidth (–3dB) is 130kHz, limited principally by C_2 and the R_{on} of S3. Full-power response is about 6kHz, limited by the slewing rates of the amplifiers, which also reduces 20V settling time to about 50µs (Figure 3). CR1 and CR2 protect the quad switches from failure if the input/output voltages exceed the power-supply. C1 provides phase compensation for stability when the loop is closed in *sample*.

DIGITALLY-CONTROLLED TIMING USING THE AD7501 MULTIPLEXER†

The circuit of Figure 4 provides digital control for variable time-delay generation. The 3 digital inputs, A_0 through A_2, select a resistor, R_1 – R_8, to provide time delays of 1-8 seconds in 1s increments. A negative transition at the 555 timer's trigger input starts the timing sequence. Additional intervals can be generated by stacking multiplexers and using their *enable* lines to select the appropriate AD7501. ▶▶▶

CODE	DELAY
000	1s
001	2s
010	3s
011	4s
100	5s
101	6s
110	7s
111	8s

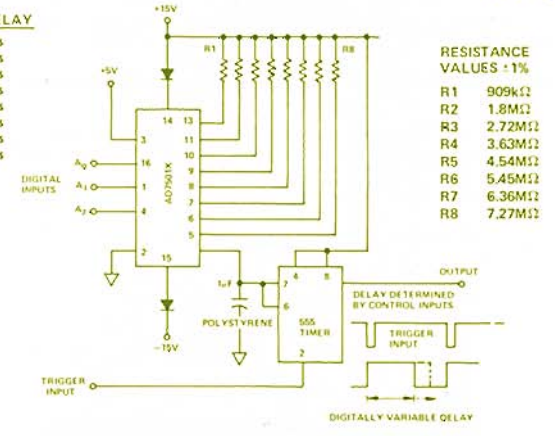


Figure 4. 8-Step digitally-controlled timer: circuit and timing diagram.

†For information on the AD7501 Multiplexer, request **L16**.

LOCK-IN AMPLIFIER USES SINGLE IC

by David R. Williams and William T. Lum*

The circuit of Figure 1, which combines a synchronous filter with a phase detector, will detect a modulated signal buried in noise. The dc output is proportional to the modulated signal, while the underlying component of noise is smoothed by the RC filter. Although the technique has been used before, the circuit described here uses a single IC instrumentation amplifier (in this case, the AD520†). The circuit was developed for multi-channel radiometry, where economical circuitry and high performance are a desirable combination, but it should find application in many fields where signal-in-noise detection is required.

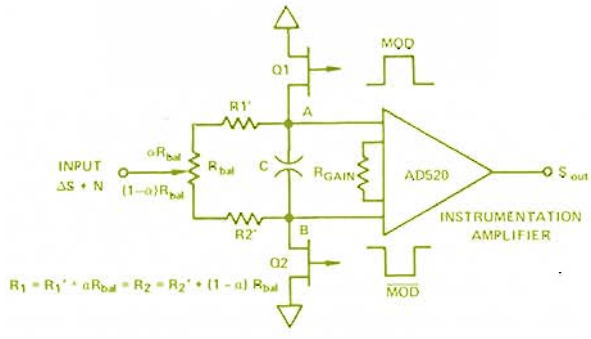


Figure 1. Synchronous demodulator

The operation of the circuit is illustrated in Figure 2. During the first half-cycle, FET Q1 is on and grounds the capacitor at A; at the same time, Q2 is off and presents a high impedance to the capacitor at B. The capacitor starts to charge up positively on the time constant R_1C. In the next half-cycle, the situation is reversed — Q2 is grounded and Q1 is open, the capacitor retains its previous charge and continues to charge negatively at B on the time constant $T = R_2C$, ($R_1 \cong R_2$). In this way, the capacitor charges up to average value $\pm\Delta S/4$,

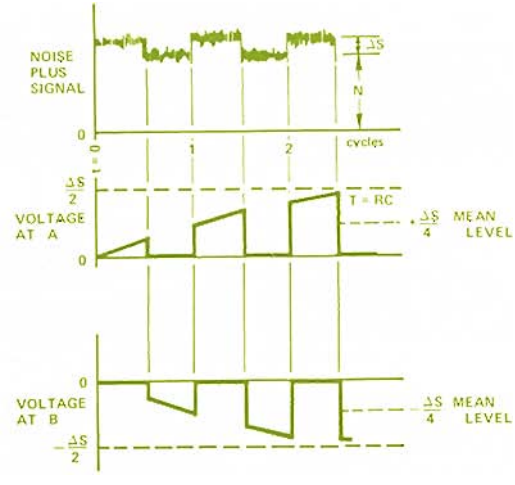


Figure 2. Waveforms at the input

which is differentially amplified to give $G_o\Delta S/2$ at the output. Only a signal which is coherent with the reference frequency will be amplified, and the random noise components will be smoothed by the RC network.

In operation, the circuit is found to have excellent zero level stability. When operating with T = 1s and $G_o = 100$, the long-term instability, noise plus drift at the output, is ≅ 1mV peak-to-peak.

The effective noise at the output can be calculated from the usual radiometer equation. For a modulated signal ΔS, masked in underlying noise N_{rms}, the signal/noise ratio at the output is given by

$$\left(\frac{S}{N}\right)_{out} = \frac{\Delta S}{N_{rms}} (\beta T)^{1/2} \qquad (1)$$

where β is the bandwidth of the band-limited noise at the input and T = RC. For example, if ΔS = 10mV, N_{rms} = 1V, β = 10kHz, T = 1s, and G_o = 100,

$$\left(\frac{S}{N}\right)_{out} = \frac{10^{-2}}{1} (10^4)^{1/2} = 1 \qquad (2)$$

and $S_{out} = G_o\Delta V_s$ = 1V. Thus, a 10mV signal masked by $1V_{rms}$ noise would just be detectable as a 1V signal at the output.

Besides its economy, there are a number of other advantages of the circuit. For example,

- The dc component of the signal-plus-noise is rejected by the amplifier's common-mode rejection (up to 120dB here).
- The use of a single capacitor across the high-impedance input of the amplifier (instead of two capacitors to common) provides improved common-mode rejection for the unwanted noise components.
- The use of a classic instrumentation amplifier provides all of its expected benefits, including symmetrical (and high) input impedance, and stable gain, determined by a single gain resistor (once the scale resistor has been selected).
- The smoothing time constant, T = RC, is determined by a single high-quality (polystyrene or polycarbonate) capacitor, given R_1, R_2. The circuit performs with reference frequencies beyond 10kHz.

In practice, in order to balance the system, a large dc signal is applied at the input, and R_{adj} is adjusted for zero dc output. This, at the same time, balances the circuit for ac symmetry ($R_1 = R_2$). ▶▶▶

*Radio Astronomy Laboratory, University of California, Berkeley, Calif. 94720.

†For information on the AD520, request **L17**.

CURRENT CONTROLLER USES ADJUSTABLE EXPONENT

by Galen W. Ewing*

In connection with electrochemical studies (variable-current chronopotentiometry), an instrument was required that would control the current i through a cell as a power of time

$$i(t) = k\,t^m$$

in which the exponent, m, can assume a wide range of values of either sign and ranging from perhaps 1/4 to 3.0.

The 433J† has proved to be a highly convenient component for accomplishing this design, using the circuit of Figure 1.

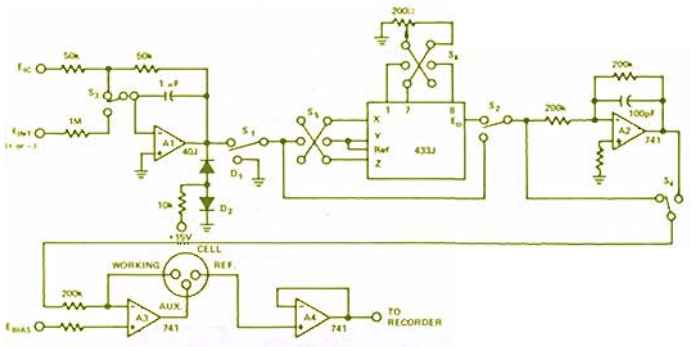


Figure 1. Power-of-time programmable galvanostat. Offset trimming and power-supply circuitry are conventional.

Two DPDT panel switches determine the sign of the exponent (S5) and whether it is greater or less than 1 (S6). The 200Ω 10-turn pot connected to S6 fixes the numerical value of the exponent, 1000 X dial setting for m < 1, and 1000 ÷ dial setting for m > 1. Switched fixed resistors could be used for a limited set of specific m values.

Two of the inputs to the 433J are fixed: the Y input, and either X or Z, as selected by S5. They are connected to the 9-volt reference output at pin 11. The active input is supplied from a conventional ramp generator utilizing a Model 40J FET-input amplifier as the integrator (A1). The integrator output is clamped to ground by diodes D1 and D2, to avoid applying negative inputs to 433 (while not harmful, negative inputs drive the output into saturation). The SPDT panel switch (S3) controls the integrator: *initial conditions* and *run; hold* is not needed. The switch is synchronized with the recorder's *remote start* control.

The 433J output (direct or inverted) is taken to a control amplifier (A3), the galvanostat proper, the feedback for which is the electrochemical cell. With the programmed current flowing through the cell, the voltage between the reference electrode and the "working" electrode is unloaded by the follower (A4) and plotted on an X-Y recorder with its X-axis driven by the linear time base. Figure 2 (adjacent column) shows the programmed current, compared with computed points for m = 3/4 and 4/3, using a 200kΩ dummy load to replace the cell for this measurement. ▶▶▶

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†See page 14.

Worth Reading

LAST ISSUE OF *ANALOG DIALOGUE*

Vol. 7 (1973), No. 2

If you haven't seen the last issue of *Dialogue*, you can get a copy by requesting **L18**. Here's what you've missed:

"SERDEX" SERial Data EXchange Modules for "No Software" Interfacing in Data Communication and Control Systems

CMOS Quad Switches and Multiplexers – Low-Leakage, Low-Dissipation Analog I.C.'s [See also p. 17 this issue]

Internally-Trimmed Monolithic Multiplier (AD532) – No External Components Required for <1% Maximum Error

Line-Operated 3½-Digit DPM (AD2006) [See also p. 15 here]

Model 50: Wideband Fast-Settling 100mA Op Amp

Model 171: High-Voltage Op Amp – Supplies to ±150V, PSR, CMR 100dB

Log-Ratio Modules (Model 756) – 0.5% Log Conformity

Applications Quickie: *Bootstrapped AC Coupling*

Erratum for Vol. 7, No. 1 – Important if You've Considered Using the AGC Circuit on p. 13 of 7–1

Editorials: On New Advances in ADI's Technology: Controlled Interfacing, Analog CMOS, Dynamically-Trimmed Monolithic IC's

Advertisements: Conversion Products, Low-Leakage Dual FET's, Fast IC Op Amps That Are Easy to Use, Three-Variable IC Multiplier-Divider ▶▶▶

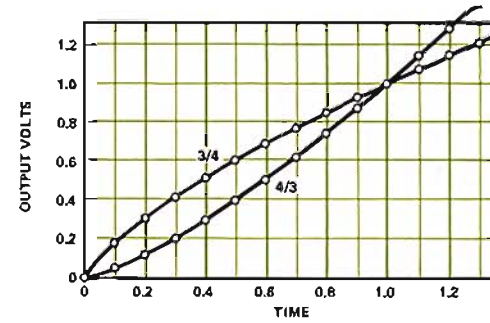

Figure 2. Power of time curves. Output voltage proportional to the 4/3 and 3/4 powers of time. Both scales normalized about the point of intersection. Circled points are calculated.

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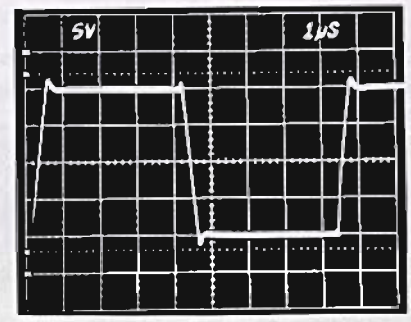
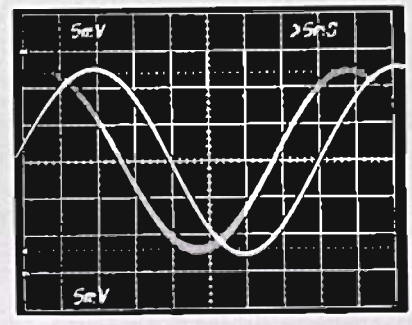


Transient response for the AD528



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